REMARKS

Claims 1-8, 10-16 and 25-26 were examined. Claims 1, 7 and 14-15 are amended. Claims 6 and 17-26 are canceled. Claims 28-29 are added. Claims 1-5, 7-16 and 28-29 remain in the application.

The Patent Office rejects claims 1-8, 10, 14-16 and 25-26 under 35 U.S.C. §102(b). The Patent Office rejects claims 11-13 under 35 U.S.C.A §103(a). Reconsideration of the rejected claims is respectfully requested in view of the above amendments and the following remarks.

A. 35 U.S.C. §102(b): Rejection of Claims 1-8, 10, 14-16 & 25-26

The Patent Office rejects claims 1-8, 10, 14-16 and 25-26 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 6,121,100 of Andideh et al. (Andideh).

Independent claims 1 and 9 are not anticipated by Andideh, because Andideh does not describe an apparatus comprising a substrate; a first device including a gate electrode on a surface of the substrate in an area of the substrate defined by a first well; a single crystal silicon alloy material disposed in each of the first junction region and the second junction region, wherein a lattice spacing of the silicon alloy material is different than a lattice spacing of a material of the well of the substrate; and a second device complementary to the first device and comprising junction regions defined by doped portions of a material of a second well of the substrate, the material of the second well of a conductivity type different than a conductivity type of the first well.

Andideh describes a method of forming a MOS transistor. Andideh does not describe forming complementary devices (e.g., NMOS and PMOS devices of a CMOS) where one device includes junction regions in a non-planar relationship with a substrate and a complementary device with junction regions defined by doped portions of a material of a well of the substrate.

With regard to claim 1, support for complementary devices may be found in the Application with reference, for example, to Figures 1-7. Paragraph 0012 at page 3 of the Application, for example, describes the devices formed with reference to Figures 1-7 as NMOS and PMOS devices of a CMOS structure. Support for a single crystal silicon alloy material may

be found in the Application, for example, at pages 10-11, paragraph 0027. Support for a silicon alloy material having a lattice spacing that is different than a lattice spacing of a material of the well of the substrate may be found in the Application, for example, at pages 8-9, paragraph 0024. Finally, support for a second device complementary to a first device and having junction regions defined by doped portions of the second well may be found in the Application, for example, at page 6, paragraph 0018.

Claims 2-5, 7-8 and 10 depend from claim 1 and therefore contain all the limitations of that claim. For at least the reasons stated with respect to claim 1, claims 2-5, 7-8 and 10 are not anticipated by Andideh.

Independent claim 14 is not anticipated by Andideh, because Andideh does not describe an apparatus including a substrate; a first device including a gate electrode on a surface of the substrate and a first junction region and a second junction region in the substrate adjacent to gate electrode; a silicon alloy material in each of the first junction region and the second junction region; a second device complementary to the first device and comprising a gate electrode on the surface of the substrate and junction regions defined by doped portions of a material in a second well of the substrate, the second well of a conductivity type different than a conductivity type of the first well. As noted above, Andideh describes a method of forming a MOS transistor, not a complementary structure where one device includes junction regions in a non-planar relationship with a substrate and a complementary device with junction regions defined by doped portions of a material of a well of the substrate.

Claims 15-16 depend from claim 14 and therefore contain all the limitations of that claim. For at least the reason state with respect to claim 14, claims 15-16 are not anticipated by Andideh.

Applicants respectfully request that the Patent Office withdraw the rejection to claims 1-5, 7-8, 10 and 14-16 under 35 U.S.C. §102(b).

B. 35 U.S.C. §103(a): Rejection of Claims 11-13

The Patent Office rejects claims 11-13 under 35 U.S.C. §103(a) as obvious over Andideh in view of U.S. Patent No. 6,878,597 of Kim (Kim). Kim is cited for disclosing silicide layers in

source and drain region and gate structure. Claims 11-13 depend from claim 1 and therefore contain all the limitations of that claim. For at least the reason stated with respect to claim 1, claims 11-13 are prima facie not obvious over the cited references. The combination of Kim with Andideh does not address the formation of complementary devices including a device selectively having a dielectric layer disposed over a surface thereof.

Applicants respectfully request that the Patent Office withdraw the rejection to claims 11-13 under 35 U.S.C. §103(a).

C. New Claims 28-29

Applicants add new claims 28 and 29 to depend from claims 1 and 14, respectively. Support for claims 28 and 29 may be found in the Application at, for example, page 15, paragraph 0039. With respect to the selective disposition of a dielectric material, Figure 7 further shows a selective disposition of dielectric material over an NMOS device.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

Respectfully submitted,
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